Patent Claims

1. A MOSFET circuit having reduced output voltage oscillations during a switch-off operation during which the current flowing through the circuit falls to zero, comprising:

- a first MOS transistor (T1) having a first number of cells,

- a second MOS transistor (T2) having a second number of cells, the second number being less than the first number and the second MOS transistor (T2) being provided with its source-drain path in parallel with the source-drain path of the first MOS transistor (T1) between a voltage source (+U) and reference-ground potential, and

- a constant voltage element (Z1) between gate of the first MOS transistor (T1) and gate of the second MOS transistor (T2).

2. The MOSFET circuit as claimed in claim 1, wherein the constant voltage element is a zener diode (Z1).

3. The MOSFET circuit as claimed in claim 1 or 2, wherein a first resistor (R2) is provided in parallel with the constant voltage element (Z1).

4. The MOSFET circuit as claimed in claim 3, wherein a second resistor (R1) is provided in series with the parallel circuit formed by the constant voltage element (Z1) and the first resistor (R2).

5. The MOSFET circuit as claimed in claim 2,

wherein
the zener diode (Z1) and the first resistor (R2) are integrated with one another.

6. The MOSFET circuit as claimed in claim 5,
wherein
the zener diode (Z1) and the first resistor (R2) are formed by a highly doped polycrystalline layer (14) of the first conduction type and a polycrystalline layer (13) of the second conduction type that is in contact with the latter.

7. The MOSFET circuit as claimed in claim 6,
wherein
the polycrystalline layer (13) of the second conduction type is located on the polysilicon gate plane of the MOSFET circuit.

8. The MOSFET circuit as claimed in one of claims 1 to 7,
wherein
the first and second MOS transistors (T1, T2) are integrated in a semiconductor body (1, 2).

9. The MOSFET circuit as claimed in claim 6 or 7,
wherein
the doping concentration of the highly doped layer (14) is less than 10^{19} charge carriers cm^{-3}.

10. The MOSFET circuit as claimed in one of claims 1 to 9,
wherein
the MOS transistors (T1, T2) are compensation components.

11. The MOSFET circuit as claimed in claim 10,
wherein
floating or nonfloating compensation regions (16) of the first conduction type are incorporated into a semiconductor body (3) of the second conduction type.

12. An integrated MOSFET circuit having reduced output voltage oscillations during a switch-off operation during which the current flowing through the circuit falls to zero, comprising:

- a first MOS transistor (T1) having a first number of cells, said transistor being integrated in a semiconductor body (1),
- a second MOS transistor (T2) having a second number of cells, said transistor being integrated in the semiconductor body (1), the second number being less than the first number and the second MOS transistor (T2) being provided with its source-drain path in parallel with the source-drain path of the first MOS transistor (T1) between a voltage source (+U) and reference-ground potential, and
- a constant voltage element (Z1) between the gate of the first MOS transistor (T1) and gate of the second MOS transistor (T2), said constant voltage element being formed as a zener diode,

wherein

the zener diode (Z1) is formed by a polycrystalline layer (13) on a polycrystalline gate plane of the MOS transistors (T1, T2) and a zone 14 provided in the polycrystalline layer (13) and having an opposite conduction type to the conduction type of the layer (13).

13. The integrated MOSFET circuit as claimed in claim 12, wherein

a resistor (R2) located in parallel with the zener diode (Z1) is formed by the pn junction between the polycrystalline layer (13) and the zone (14).

14. The integrated MOSFET circuit as claimed in claims 12 and 13,

wherein

the doping concentration of the zone (14) is less than 10^{19} charge carriers cm^{-3}.